

DISCRETE-TIME AMPLITUDE CONTROL OF VOLTAGE-CONTROLLED
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DISCRETE-TIME AMPLITUDE CONTROL OF VOLTAGE-CONTROLLED
OSCILLATOR

TECHNICAL FIELD OF THE INVENTION

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[0001] The present invention is directed, in general, to
high performance frequency synthesizers and, more
specifically, to low phase noise voltage-controlled
oscillators suitable for use in high performance frequency
10 synthesizers.

BACKGROUND OF THE INVENTION

[0002] Voltage-controlled oscillators (VCOs) within portable communication devices such as mobile telephones and other wireless devices, must exhibit low phase noise by having the largest possible signal amplitude while ensuring that devices operate within the maximum permissible voltage amplitudes. Operating the devices within voltage limits helps to increase device reliability as well as minimize the noise generated in the active devices.

[0003] Continuous-time amplitude control for voltage-controlled oscillators has been proposed, but requires a trade-off between speed of operation and phase noise degradation resulting from low frequency bias modulation within the amplitude control loop. In addition, temperature and fabrication process variations constrain phase noise performance.

[0004] There is, therefore, a need in the art for improved amplitude control within a voltage controlled oscillator.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, wherein like numbers designate like objects, and in which:

[0006] FIGURE 1 depicts a wireless communications system employing a phase lock loop-based frequency synthesizer with a voltage-controlled oscillator with discrete-time amplitude control according to one embodiment of the present invention; and

[0007] FIGURE 2 depicts in greater detail a voltage-controlled oscillator with discrete-time amplitude control according to one embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0008] To address the above-discussed deficiencies of the prior art, it is a primary object of the present invention to provide, for use in a transceiver for a wireless communications system, a mechanism that, periodically, compares the sensed amplitude for the output signal of a voltage-controlled oscillator to a reference and sets biasing of the voltage-controlled oscillator is correspondingly, thereby controlling amplitude of the voltage-controlled oscillator output signal. Process and temperature dependencies of the amplitude are eliminated while achieving low phase noise and large signal-to-noise ratio in the output signal, and consequently low phase noise.

[0009] The foregoing has outlined rather broadly the features and technical advantages of the present invention so that those skilled in the art may better understand the detailed description of the invention that follows. Additional features and advantages of the invention will be described hereinafter that form the subject of the claims of the invention. Those skilled in the art will appreciate that they may readily use the conception and the specific embodiment disclosed as a basis for modifying or designing

other structures for carrying out the same purposes of the present invention. Those skilled in the art will also realize that such equivalent constructions do not depart from the spirit and scope of the invention in its broadest form.

[0010] Before undertaking the DETAILED DESCRIPTION OF THE INVENTION below, it may be advantageous to set forth definitions of certain words or phrases used throughout this patent document: the terms "include" and "comprise," as well as derivatives thereof, mean inclusion without limitation; the term "or" is inclusive, meaning and/or; the phrases "associated with" and "associated therewith," as well as derivatives thereof, may mean to include, be included within, interconnect with, contain, be contained within, connect to or with, couple to or with, be communicable with, cooperate with, interleave, juxtapose, be proximate to, be bound to or with, have, have a property of, or the like; and the term "controller" means any device, system or part thereof that controls at least one operation, whether such a device is implemented in hardware, firmware, software or some combination of at least two of the same. It should be noted that the functionality associated with any particular controller may be centralized or distributed, whether locally or remotely.

Definitions for certain words and phrases are provided throughout this patent document, and those of ordinary skill in the art will understand that such definitions apply in many, if not most, instances to prior as well as
5 future uses of such defined words and phrases.

[0011] FIGURES 1 and 2, discussed below, and the various embodiments used to describe the principles of the present invention in this patent document are by way of illustration only and should not be construed in any way to
10 limit the scope of the invention. Those skilled in the art will understand that the principles of the present invention may be implemented in any suitably arranged device.

[0012] FIGURE 1 depicts a wireless communications system
15 employing a phase lock loop-based frequency synthesizer with a voltage-controlled oscillator with discrete-time amplitude control according to one embodiment of the present invention. Wireless communications system 100 includes a transmitter 101 and receiver 102 (or transceiver
20 pair), and at least one communications channel 103 communicably coupling the transmitter 101 and receiver 102. Wireless communications system 100 may be employed for voice communications, video transmission or data transmission. Accordingly, receiver (or transceiver) 102 may

be, for example, a mobile telephone, a satellite or terrestrial television receiver, a data processing system such as a wireless personal digital assistant (PDA) with Internet access capabilities, or some combination thereof.

5 [0013] Those skilled in the art will recognize that the complete structure and operation of a wireless communications system or a receiver therein are not depicted or described herein. Instead, for simplicity and clarity, only so much of a wireless communications system and
10 associated receiver as is unique to the present invention or necessary for an understanding of the present invention is depicted and described.

[0014] A phase lock loop (PLL)-based frequency synthesizer 104 is commonly used in communication and
15 control systems. The frequency synthesizer 104 provides a programmable, highly stable signal of the desired frequency, phase noise and power level. The frequency synthesizer 104 consists of a high quality, low-frequency external quartz crystal oscillator 105 whose output signal
20 is the reference to the phase lock loop 106. That reference signal is used to derive a higher frequency signal through frequency multiplication. The error between the reference signal and the actual synthesized frequency output signal is detected by a phase detector 107 and

averaged through a low-pass filter (LPF) 108. The averaged signal forms the control input to a voltage-controlled oscillator 109, with a frequency divider (counter) 110 within the feedback loop.

5 [0015] Phase noise characteristics of the frequency synthesizer for frequencies greater than the PLL loop bandwidth (with respect to the synthesized carrier frequency) is determined by the phase noise of the VCO 109. The requirement for low phase noise at offset frequencies
10 greater than the loop bandwidth is very important for receiver and transmitter performance in wireless communications systems. In the present invention, the voltage-controlled oscillator 109 employs discrete-time amplitude control as described in further detail below.
15 Additionally, while frequency synthesizer 104 is depicted within the transmitter 101 within the exemplary embodiment of FIGURE 1, the same structure may also be implemented within receiver 102.

[0016] FIGURE 2 depicts in greater detail a voltage-
20 controlled oscillator with discrete-time amplitude control according to one embodiment of the present invention. Voltage-controlled oscillator and control system 200 includes an inductive-capacitive (L-C) voltage-controlled oscillator 201, bias controller 202 for biasing the

voltage-controlled oscillator 201 and thereby controlling the gain and the amplitude of the output signal from the voltage-controlled oscillator 201, and a discrete-time amplitude controller 203 passing amplitude control signals to the bias controller 202 on an amplitude control signal bus 204.

[0017] In the exemplary embodiment, differential voltage-controlled oscillator 201 includes an L-C tank circuit formed by identical inductors L_1 and L_2 , capacitors C_{T1} and C_{T2} , and voltage-controlled varactor C_v , together with cross-coupled transistors Q_1 and Q_2 and feedback capacitive voltage dividers C_{11} , C_{12} and C_{21} , C_{22} from the L-C tank to the transistors Q_1 and Q_2 . Inductors L_1 and L_2 are both connected at one end to a power supply voltage VDD and at the other end to one terminal of varactor C_v , with the connections between the inductors L_1 and L_2 and varactor C_v forming the output nodes T_N and T_P of the L-C tank.

[0018] Voltage dividers C_{11} , C_{12} and C_{21} , C_{22} are connected between output nodes T_P and T_N , respectively, and a ground voltage GND. The base of transistor Q_1 is connected to the junction between capacitors C_{11} and C_{12} , and the base of transistor Q_2 is connected to the junction between capacitors C_{21} and C_{22} . Also connected to the junction between capacitors C_{11} and C_{12} is one end of resistor R_1 , and

connected to the junction between capacitors C_{21} and C_{22} is one end of resistor R_2 . The other ends of resistors R_1 and R_2 are connected to a voltage generated by voltage bias circuit VBIAS within bias circuitry 202.

5 [0019] Inductors L_1 and L_2 , capacitors C_{T1} and C_{T2} , transistors Q_1 and Q_2 , capacitors C_{11} and C_{21} , capacitors C_{12} and C_{22} , and resistors R_1 and R_2 are each respectively matched in size and electrical characteristics. While a push-pull configuration for the voltage-controlled
10 oscillator 201 is employed in the exemplary embodiment, the present invention may be implemented within published VCO topologies for either single-ended or differential operation, with bipolar junction transistors, metal-oxide-semiconductor transistors, or any other active devices that
15 provide the negative transconductance to compensate for losses within the L-C tank.

[0020] Through resistors R_1 and R_2 , transistors Q_1 and Q_2 are biased at the direct current voltage set by circuit VBIAS within bias circuitry 202. Circuit IBIAS in the
20 exemplary embodiment contains N parallel current sources that are individually enabled by enable signals EN_1 through EN_N , with transistors Q_1 and Q_2 biased at current levels set by circuit IBIAS. Accordingly, for given inductances of inductors L_1 and L_2 and capacitances of capacitors C_{T1} , C_{T2} ,

C_v , C_{11} , C_{21} , C_{12} and C_{22} , the amplitude of the tank signal at the output nodes T_N and T_P is determined by the voltage set by circuit VBIAS and the current set by circuit IBIAS. The frequency of the voltage-controlled oscillator 201 is
5 determined by (a) the inductance of inductors L_1 and L_2 and (b) the net capacitance at the output nodes T_N and T_P , which varies based on the capacitance of varactor C_v .

[0021] Bias circuitry 202 includes VBIAS and IBIAS cells. Circuit IBIAS sets the tail current of the coupled-emitter, cross-coupled transistor pair Q_1 and Q_2 and may be
10 a set of current mirrors as depicted or a set of switchable resistors. Circuit VBIAS sets the direct current base voltage which controls the switching interval of the cross-coupled transistors Q_1 and Q_2 and the operating region of
15 the IBIAS cell, and therefore control the current through the transistors Q_1 and Q_2 .

[0022] Amplitude control circuitry 203 includes a tank output amplitude sense circuit 205 receiving the differential output from output nodes T_N and T_P sensing the
20 tank amplitude and generating a signal representative of the output amplitude from L-C tank voltage-controlled oscillator 201 and a tank amplitude reference circuit 206 generating a signal representative of the desired tank amplitude. Comparator 207 periodically compares the out-

puts of tank amplitude sense circuit 205 and tank amplitude reference circuit 206, triggered by a clock signal CLK.

[0023] The output of the comparator 207 (a high or low signal) is processed by a logic state machine 208 implementing algorithms ensuring that (a) the voltage-controlled oscillator 201 has the minimum current required for start up, and (b) the VBIAS and IBIAS cells are switched to provide the desired values of bias quantities such that the desired tank amplitude is obtained. Voltage-controlled oscillator tank amplitude control state machine 208 controls the VBIAS and IBIAS circuits via tank amplitude control signal bus 204. State machine 208 updates the control signals on tank amplitude control signal bus 204 on a periodic basis, triggered by clock signal CLK.

[0024] The present invention employs a tank voltage sense circuit, a reference tank voltage signal, and a clocked comparator to compare the sensed and reference signals, and a clocked state machine employing an algorithm to increase or decrease the tank bias current and voltage in discrete steps. Unlike a continuous-time sensing and amplitude control scheme, the discrete-time amplitude control scheme of the present invention does not involve an inherent trade-off between speed of operation and phase noise degradation due to low-frequency bias modulation.

[0025] The amplitude control scheme of the present invention operates during the calibration phase. After completion of the calibration phase, the oscillator bias conditions are held constant. However, the amplitude control operation may be performed as frequently as desired to eliminate both process and temperature dependencies of the voltage-controlled oscillator tank amplitude.

[0026] The discrete-time amplitude control system of the present invention obtains the lowest possible phase noise within a voltage-controlled oscillator with the largest possible signal-to-noise ratio within the L-C tank signal, biasing the tank such that the largest possible signal subject to biasing is obtained and operating the various active devices in their low-noise region. The oscillator operates in the mode described without introduction by the amplitude control scheme of any mechanisms causing degradation of the oscillator phase noise, as found in continuous-time amplitude control feedback schemes. Accordingly, the present invention achieves the best possible phase noise over fabrication process and temperature variation without phase noise degradation due to modulation of bias by the amplitude control loop.

[0027] Although the present invention has been described in detail, those skilled in the art will understand that

various changes, substitutions, variations, enhancements, nuances, gradations, lesser forms, alterations, revisions, improvements and knock-offs of the invention disclosed herein may be made without departing from the spirit and scope of the invention in its broadest form.

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